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A Family of Five-Level Dual-Buck Full-bridge Inverters for Grid-tied Applications

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***Abstract*—Dual-buck inverters feature some attractive merits, such as no reverse recovery issues of the body diodes and free of shoot-through. However, since the filter inductors of dual-buck inverters operate at each half cycle of the utility grid alternately, the inductor capacity of dual-buck inverters is twice as much as H-bridge inverters. Thus, the power density of dual-buck converters needs to be improved, as well as the conversion efficiency. In this paper, the detailed derivation process of two five-level full-bridge topology generation rules are presented and explained. One is the combination of a conventional three-level full-bridge inverter, a two-level capacitive voltage divider and a neutral point clamped (NPC) branch. The other method is to combine a three-level half-bridge inverter and a two-level half-bridge inverter. Furthermore, in order to enhance the reliability of existing five-level DBFBI topologies, an extended five-level DBFBI topology generation method is proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter, thus a family of five-level DBFBI topologies with high reliability is proposed. The operation modes, modulation methods and control strategies of the series-switch five-level DBFBI topology are analyzed in detail. The power device losses of the three-level DBFBI topology and five-level DBFBI topologies, with different switching frequencies, are calculated and compared. Both the relationship between the neutral point potential self-balancing and the modulation index of inverters are revealed. A universal prototype was built up for the experimental tests of the three-level DBFBI topology, the five-level H-bridge inverter topology and the existing three five-level DBFBI topologies. Experimental results have shown that the five-level DBFBI topologies exhibit higher efficiency than the five-level H-bridge inverter topology and the three-level DBFBI topology. As well, the higher power density has been achieved by the five-level DBFBI topologies compared with the three-level DBFBI topology.**

***Index Terms*—Grid-tied inverter, Dual-buck inverter, Multi-level inverter, Efficiency, Power density**

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I. Introduction

The demand for renewable generation has increased significantly over the past years because of the considerations on fossil fuel shortage and greenhouse effect. Among various types of renewable generation, photovoltaic generation, wind generation, and fuel cells have been widely utilized [1]-[5], and the grid-tied inverters are key elements in renewable generation systems to interface the renewable sources and the utility grid. Therefore, they should be careful designed to achieve high efficiency and high power density.

Power MOSFETs have some attractive advantages, such as fast switching, low switching loss and resistive conduction voltage drop. The switching frequency of the power converters using MOSFETs can be higher than that of the power converters using IGBTs, which benefits for reducing current ripples and the size of passive components. However, since the reverse recovery characteristic of the body diodes is poor, power MOSFETs cannot be used in conventional H-bridge inverters. In order to utilize the advantages of MOSFETs, soft-switching techniques are adopted conventionally [6]. However, additional auxiliary switches, passive components, and more gate driving circuits are required in the soft-switching inverter, which lowers the reliability and increases the cost and complexity. In dual-buck inverters, no reverse recovery problem occurs in the freewheeling mode, since the independent freewheeling diode has excellent reverse recovery characteristic. In addition, power MOSFETs are used in dual-buck inverters. Therefore, the dual-buck inverter is an attractive solution to achieve high efficiency for low power grid-connected applications. Many dual-buck inverter topologies have been developed in recent years [7]-[15], and some of them are utilized as grid-tied inverters. Two filter inductors are required in single-phase dual-buck inverters, and both of the inductors are operating at each half cycle of the utility grid alternately, which increases the size and weight of the converter. Hence, the power density of conventional two-level and three-level dual-buck inverters needs to be improved.

The multilevel technique is an effective way to achieve high power density. However, the number of power switches used in the multilevel inverter is more than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is much more complicated. Thus, the trade-off

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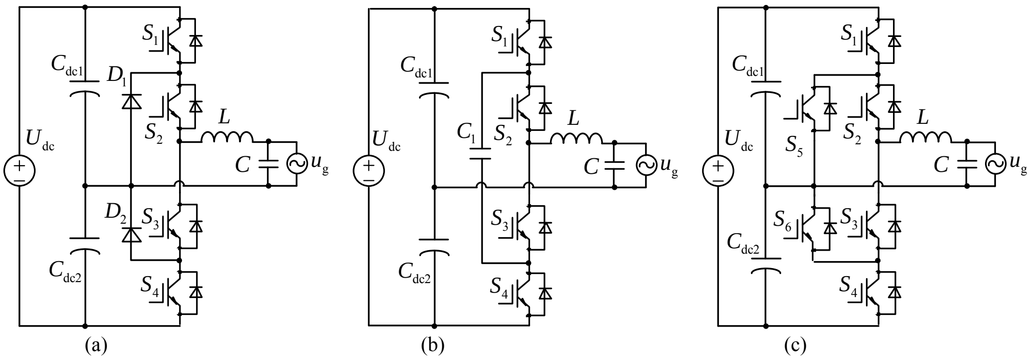

Fig.1. Three popular topologies of H-bridge multilevel inverters. (a) Diode neutral point clamped (DNPC). (b) Flying capacitor clamped(FCC). (c) Active neutral point clamped (ANPC).

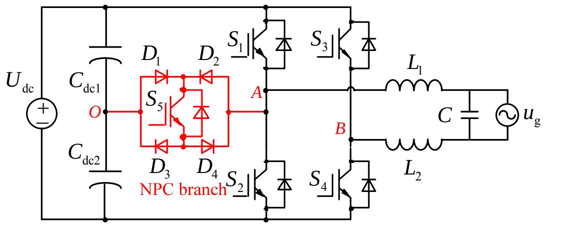

Fig.2. The simplified five-level H-bridge inverter topology [24]

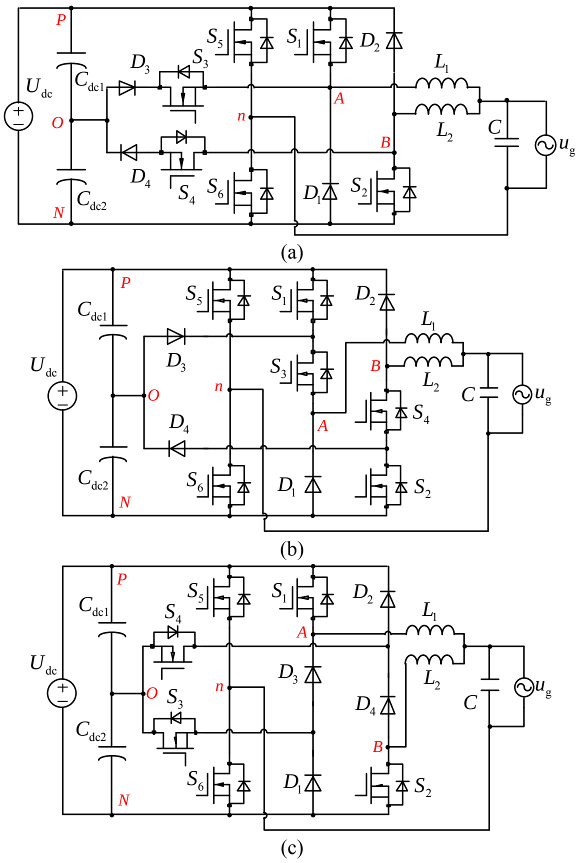

Fig.3. Three topologies of five-level DBFBIs proposed in [27]. (a). NPC five-level DBFBI. (b). Series-switch five-level DBFBI. (c). Series-diode five-level DBFBI.

between the performance and the hardware cost should be considered in the design of multilevel inverters [16]. There are three widely used topologies of single-phase multilevel inverters, as show as in Fig.1, diode neutral point clamped (DNPC) multilevel inverters [17], [18], flying capacitor clamped (FCC) multilevel inverters [19], [20], and active neutral point clamped (ANPC) multilevel inverters [21], [22]. The basic concept of the above three multilevel topologies is to use smaller rating power devices to generate appreciable high-level output voltage waveforms. However, conventional multilevel inverters require a large number of power devices and auxiliary dc links when the output voltage levels are higher than three-level.

A five-level H-bridge inverter topology was proposed by introducing a neutral point clamped bi-directional switch (NPC branch) based on the conventional full-bridge inverter [23], [24], as shown in Fig.2. Comparing with the DNPC five-level inverter topology, the FCC five-level inverter topology, and the ANPC five-level inverter topology, the number of power devices in the new five-level H-bridge inverter has been reduced significantly [24]. Therefore, for the low-voltage (less than 1000V) applications, this five-level H-bridge inverter topology is a better option than conventional multilevel inverter topologies. It is regarded as one of the best solutions for grid-tied inverters as well [16], [25], [26]. In [24], the issue of neutral point (NP) potential balancing was discussed as well, and the NP potential self-balancing of two capacitors was considered to be automatically realized. However, the NP potential self-balancing of five-level full bridge inverters is related to the modulation index.

On the other hand, three topologies of five-level dual-buck full-bridge inverters were proposed in [27], as shown in Fig.3. However, the derivation process of the proposed topologies has not been explained in detail, and the topology generation rules can also be extended. Furthermore, both the efficiency and the THD performance of the presented three five-level DBFBI topologies have never been analyzed and compared.

In this paper, the detailed derivation processes of two five-level full-bridge topology generation rules are presented and explained. An extended topology generation method is proposed for generating five-level dual-buck full-bridge inverter (DBFBI) topologies, and a family of five-level DBFBI topologies with high reliability is derived. Furthermore, the relationship between the NP potential self-balancing and the modulation index of inverters are revealed.

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This paper is organized as follows. In Section II, two topology generation rules of the five-level DBFBI topologies are presented and explained in detail. An extended topology generation method is proposed, and a family of five-level DBFBI topologies with high reliability is generated. In Section III, the series-switch five-level DBFBI topology is taken as an example for analysis in terms of the operation principle and the modulation method. The issue of neutral point (NP) potential balancing is discussed as well. In Section IV, the calculation process of power devices losses is presented, and the power devices losses comparison between the five-level DBFBI topology and the three-level DBFBI topology is given. Experimental results are shown in Section V, and Section VI concludes the paper.

II. A Family of Five-level DBFBIs Derived by Topology Generation Rules

A. The review of topology generation rules

From Fig.2, the NPC branch is formed by the switch S_5 and four diodes, D_1 to D_4. The node of the left arm A is connected with the node O (NP of the DC link) through the NPC branch. The topology generation rules of the simplified five-level H-bridge inverter can be summarized as follows.

Rule#1: The conventional three-level full-bridge inverter is combined with a two-level capacitive voltage divider and a NPC branch, as shown in Fig.4(a). The nodes of the capacitive voltage divider P_1, N_1 and O_1 are connected to the nodes of the three-level full-bridge inverter, P_2, N_2 and O_2, respectively. The node of the NPC branch O_3 is connected to the node of the three-level full-bridge inverter A. Finally, the redundant capacitors, C_{dc1} and C_{dc2}, are removed. Hence, the simplified five-level H-bridge inverter has been obtained. This topology generation rule is presented in [24], and can be applied to generate any number of voltage levels as well.

Rule#2: The simplified five-level H-bridge inverter can also be constructed by combining a three-level half-bridge inverter (Conergy topology) and a two-level half-bridge inverter, as shown in Fig.4(b). The nodes of the three-level half-bridge inverter, P_1, N_1 and O_1, are connected to the nodes of the two-level half-bridge inverter, P_2, N_2 and O_2, respectively. The node of the three-level half-bridge inverter O_1 is disconnected from the node of the utility grid n_1. The node of the two-level half-bridge inverter O_2 is disconnected from the node of the utility grid n_2. Then, the nodes, n_1 and n_2, are connected with each other.

Hence, the simplified five-level H-bridge inverter topology can be generated by two topology generation methods, and this derivation process of the simplified five-level H-bridge inverter topology was not presented in [27].

B. The NPC five-level DBFBI topology

By employing the topology generation rule #1, a three-level DBFBI topology is combined with a two-level capacitive voltage divider and a NPC branch, as shown in Fig.5(a). The nodes of the capacitive voltage divider, P_1, N_1 and O_1, are connected to the nodes, P_2, N_2 and O_2, respectively. The node of the NPC branch A_1 is connected to the node of the three-level DBFBI A_2. The node of the NPC branch B_1 is connected to the node of the three-level DBFBI B_2. Then, the redundant capacitors, C_{dc1} and C_{dc2}, can be removed. As a result, a NPC five-level DBFBI topology is generated, as shown in Fig.3.

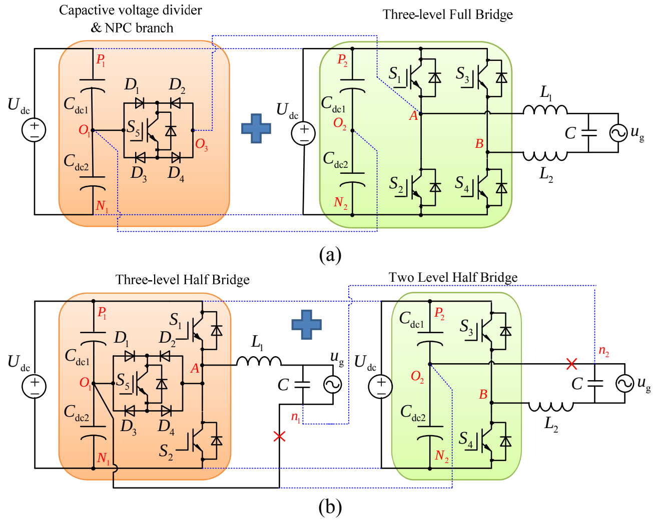

Fig.4. The topology generation rules of the simplified five-level H-bridge inverter. (a) Three-level full-bridge inverter combined with a two-level capacitive voltage divider and a NPC branch. (b) Three-level half-bridge inverter combined with a two-level half-bridge inverter.

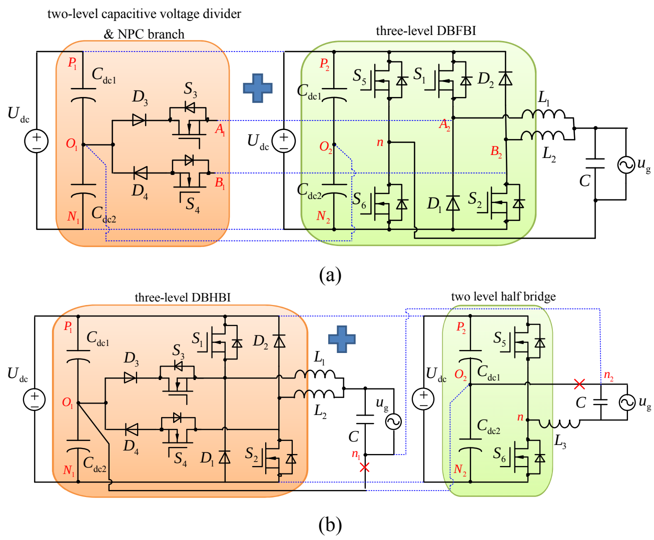

Fig.5. The topology generation rules of the proposed NPC five-level DBFBI topology. (a) A three-level DBFBI combined with a two-level capacitive voltage divider and a NPC branch. (b) A three-level DBHBI combined with a two-level half-bridge inverter.

On the other hand, a three-level DBFBI can be combined with a two-level half-bridge inverter by employing the topology generation rule #2, as shown in Fig.5(b). The nodes of the three-level DBHBI, P_1, N_1 and O_1, are connected to the nodes, P_2, N_2 and O_2, respectively. The node of the three-level DBHBI O_1 is disconnected from the node of the utility grid n_1. The node of the two-level half-bridge inverter O_2 is

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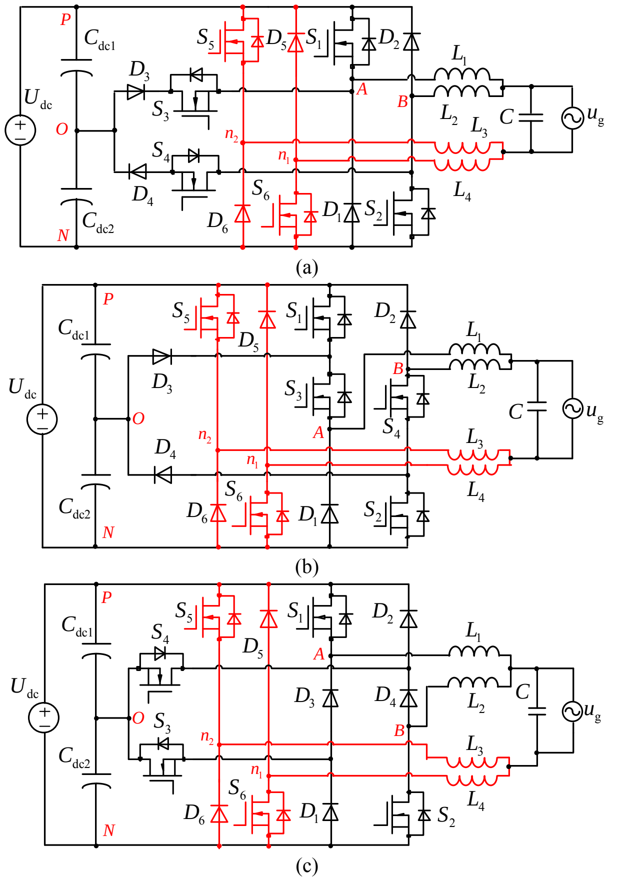

Fig.6. Three topologies of five-level DBFBIs with high reliability. (a). NPC five-level DBFBI. (b) Series-switch five-level DBFBI. (c) Series-diode five-level DBFBI.

disconnected from the node of the utility grid n_2. Then, the nodes, n_1 and n_2, are connected with each other. The redundant capacitors, C_{dc1} and C_{dc2}, and the redundant inductor L_3 are removed.

Therefore, the NPC five-level DBFBI topology can be derived from the two generation rules mentioned above. Compared with the three-level DBFBI topology (part of Fig.5(a)), there are two additional switches and two additional diodes in the proposed NPC five-level DBFBI topology.

C. An extended topology generation rule and the other five-level DBFBI topologies

In order to enhance the reliability of five-level DBFBI topologies, the two-level half-bridge inverter can be replaced by a two-level dual-buck half-bridge inverter. As a result, a family of five-level DBFBI topologies with high reliability is generated, as shown in Fig.6.

The NPC five-level DBFBI topology with high reliability, as shown in Fig.6(a), is derived from a NPC three-level DBHBI combined with a two-level dual-buck half-bridge inverter. The series-switch five-level DBFBI topology with high reliability, as shown in Fig.6(b), is derived from a series-switch three-level DBHBI combined with a two-level dual-buck half-bridge inverter. Similarly, the series-diode five-level DBFBI, as shown in Fig.6(c), is derived from a series-diode three-level DBHBI combined with a two-level dual-buck half-bridge inverter.

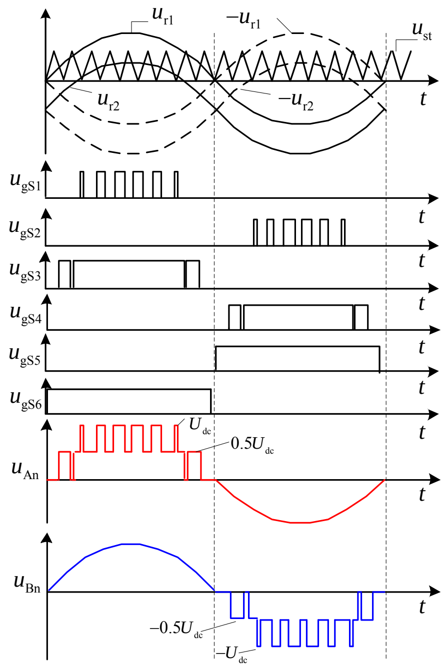

Fig.7. Key waveforms of the series-switch five-level DBFBI topology.

Therefore, a family of five-level DBFBI topologies with high reliability can be generated by employing the extended topology generation rule. Although the proposed high reliability five-level DBFBI topologies are different from the topologies proposed in [27], the modulation methods and the operation modes are similar. The total inductance of split inductors (L_1 and L_4) in high reliability five-level DBFBI topologies is the same as that of the inductor L_1 in five-level DBFBI topology. However, since there are two additional diodes, the hardware cost of the proposed high reliability topologies is higher. Therefore, the following analyses on switching states, neutral point (NP) potential balancing, and power devices losses are conducted based on the five-level DBFBI topologies presented in [27].

III. Analysis on the Series-Switch Five-Level DBFBI Topology

A. Switching State Analysis

The Series-switch five-level DBFBI topology is taken as an example for detailed analysis. The key waveforms of the Series-switch five-level DBFBI are shown in Fig.7.

Two reference signals, u_{r1} and u_{r2}, are compared with a carrier signal u_{st} to produce pulse width modulation (PWM) signals for the switches. u_{gS1} to u_{gS6} represent the gate drive signals of power switches S_1 to S_6. In order to avoid the shoot-through problem, the dead time has been set within the drive signals of the switches S_5 and S_6. u_{An} represents the voltage difference between the node A and node n, and u_{Bn} is the voltage difference between the node B and node n. Two filter inductors, L_1 and L_2, are operating at each half cycle of the

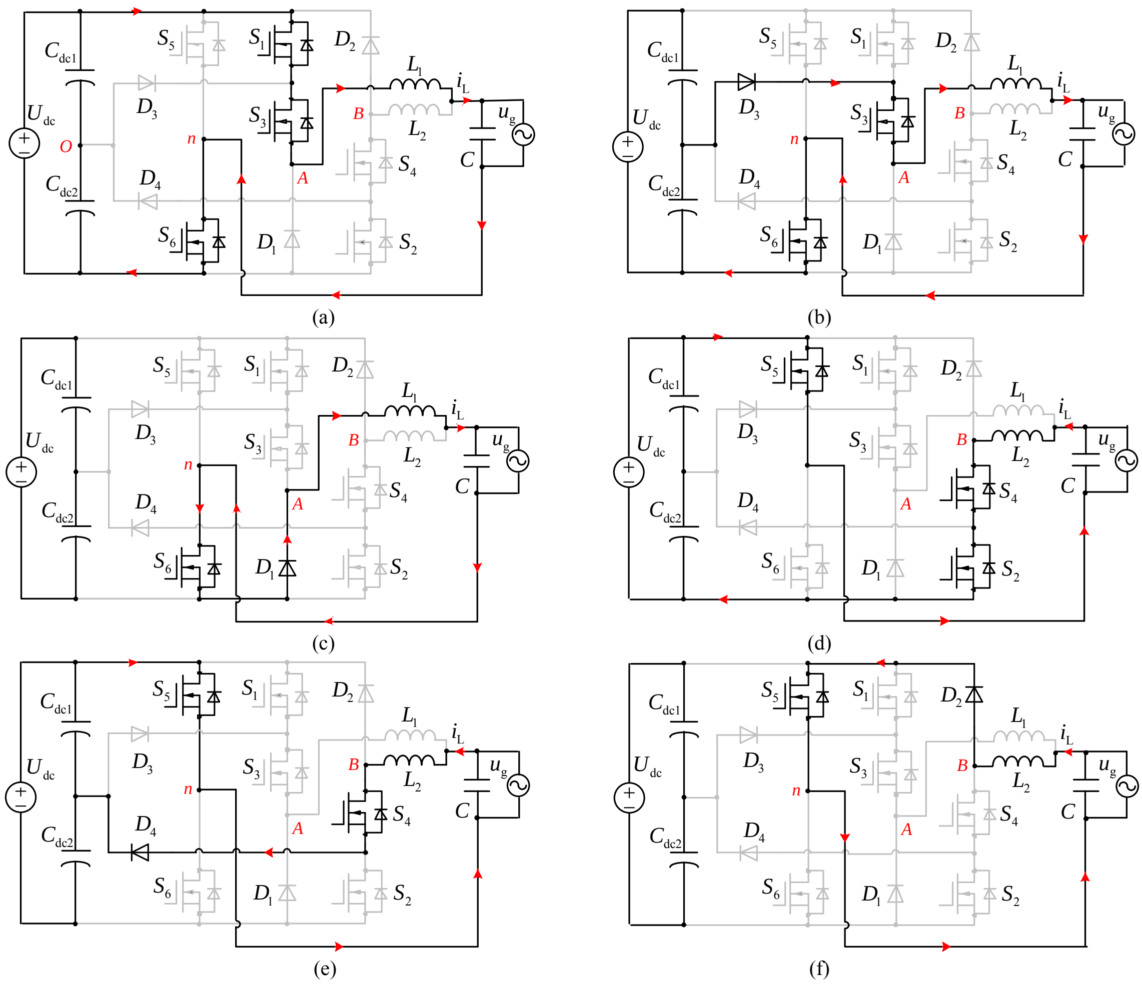

Fig.8. Equivalent circuits of switching state. (a) State #1. (b) State #2. (c) State #3. (d) State #4. (e) State #5. (f) State #6.

utility grid alternately. Therefore, $u_{\text{AB-n}}$ is defined as the output levels of the DBFBI topologies, and $u_{\text{AB-n}}$ is represented as,

$$u_{\text{AB-n}} = u_{\text{An}} + u_{\text{Bn}} - u_{\text{g}} \tag{1}$$

On the other hand, the series-switch five-level DBFBI topology is operating with unity power factor. In order to avoid the inductor current distortion, at the beginning of the positive half cycle of the utility grid, the switches S_1, S_3 and S_6 are turned ON at the same time. At the end of the positive half cycle, the switch S_3 is turned OFF before the switch S_6, and the current of inductor L_1 decreases to zero naturally. Similarly, at the beginning of the negative half cycle of the utility grid, the switches S_2, S_4 and S_5 are turned ON at the same time. At the end of the negative half cycle, the switch S_4 is turned OFF before the switch S_5, and the current of inductor L_2 decreases to zero naturally. Since the series-switch five-level DBFBI topology is digitally controlled, this modulation method is easy to implement. Furthermore, it is also suitable to both the NPC five-level DBFBI topology, the series-diode five-level DBFBI topology, and the family of five-level DBFBI topologies with high reliability. The series-switch five-level DBFBI has six operation modes, which are shown in Fig.8.

(1) *State #1* [*Refer to Fig.8(a)*]. Maximum positive output, $u_{\text{An}}=U_{\text{dc}}$. There is no current flowing through the inductor L_2, thus the voltage on the inductor L_2 is equal to zero, and $u_{\text{Bn}}=u_{\text{g}}>0$. As a result, $u_{\text{AB-n}}=U_{\text{dc}}$. S_1, S_3 and S_6 are turned ON, and the other switches are turned OFF. The active current path at this state is shown in Fig.8(a). The reverse blocking voltage on D_3 is equal to $0.5U_{\text{dc}}$, and the reverse blocking voltage on D_1 is equal to U_{dc}. The drain-source voltage on S_5 is equal to U_{dc}. During this state, the inductor current i_{L1} increases linearly,

$$L_1 \frac{di_{\text{L1}}}{dt} = U_{\text{dc}} - u_{\text{g}} \tag{2}$$

(2) *State #2* [*Refer to Fig.8(b)*]. Half-level positive output, $u_{\text{An}}=0.5U_{\text{dc}}$. There is no current flowing through the inductor L_2, thus the voltage on the inductor L_2 is equal to zero, and $u_{\text{Bn}}=u_{\text{g}}>0$. As a result, $u_{\text{AB-n}}=0.5U_{\text{dc}}$. S_3 and S_6 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.8(b). The drain-source voltage on S_1 is equal to $0.5U_{\text{dc}}$, and the reverse blocking voltage on D_1 is equal to $0.5U_{\text{dc}}$. During this state, the inductor current i_{L1} decreases linearly when the voltage of the utility grid is higher than $0.5U_{\text{dc}}$,

$$-L_1 \frac{di_{\text{L1}}}{dt} = \frac{U_{\text{dc}}}{2} - u_{\text{g}} \tag{3}$$

The inductor current i_{L1} increases linearly when the voltage of the utility grid is lower than $0.5U_{\text{dc}}$,

$$L_1 \frac{di_{L1}}{dt} = \frac{U_{dc}}{2} - u_g \tag{4}$$

(3) *State #3* [*Refer to Fig.8(c)*]. Zero output at the positive half period of the utility grid, u_{An}=0. There is no current flowing through the inductor L_2, thus the voltage on the inductor L_2 is equal to zero, and $u_{Bn}=u_g>0$. As a result, u_{AB-n}=0. S_6 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.8(c). Both the drain-source voltages on S_1 and S_3 are equal to $0.5U_{dc}$. During this state, the inductor current i_{L1} decreases linearly,

$$L_1 \frac{di_{L1}}{dt} = -u_g \tag{5}$$

(4) *State #4* [*Refer to Fig.8(d)*]. Zero output at the negative half period of the utility grid, u_{Bn}=0. There is no current flowing through the inductor L_1, thus the voltage on the inductor L_1 is equal to zero, and $u_{An}=u_g<0$. As a result, u_{AB-n}=0. S_5 is turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.8(d). Both the drain-source voltages on S_2 and S_4 are equal to $0.5U_{dc}$. During this state, the inductor current i_{L2} increases linearly,

$$L_2 \frac{di_{L2}}{dt} = -u_g \tag{6}$$

(5) *State #5* [*Refer to Fig.8(e)*]. Half-level negative output, $u_{Bn}=-0.5U_{dc}$. There is no current flowing through the inductor L_1, thus the voltage on the inductor L_1 is equal to zero, and $u_{An}=u_g<0$. As a result, $u_{AB-n}=-0.5U_{dc}$. S_4 and S_5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.8(e). The drain-source voltage on S_2 is equal to $0.5U_{dc}$, and the reverse blocking voltage on D_2 is equal to $0.5U_{dc}$. During this state, the inductor current i_{L2} decreases linearly when the voltage of the utility grid is lower than $0.5U_{dc}$,

$$-L_2 \frac{di_{L2}}{dt} = -\frac{U_{dc}}{2} - u_g \tag{7}$$

The inductor current i_{L2} increases linearly when the voltage of the utility grid is higher than $0.5U_{dc}$,

$$L_2 \frac{di_{L2}}{dt} = -\frac{U_{dc}}{2} - u_g \tag{8}$$

(6) *State #6* [*Refer to Fig.8(f)*]. Maximum negative output, $u_{Bn}=-U_{dc}$. There is no current flowing through the inductor L_1, thus the voltage on the inductor L_1 is equal to zero, and $u_{An}=u_g<0$. As a result, $u_{AB-n}=-U_{dc}$. S_2, S_4 and S_5 are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig.8(f). The reverse blocking voltage on D_4 is equal to $0.5U_{dc}$, and the reverse blocking voltage on D_2 is equal to U_{dc}. During this state, the drain-source voltage on S_6 is equal to U_{dc}. In this mode, the inductor current i_{L2} decreases linearly,

$$-L_2 \frac{di_{L2}}{dt} = -U_{dc} - u_g \tag{9}$$

Based on the equations (2) to (9), it can be seen that the voltage jump of filter inductors is $0.5U_{dc}$, and the duty cycles of switches, S_1 to S_4, can be derived as,

TABLE I.
THE MAXIMUM VOLTAGE STRESSES OF THE POWER DEVICES IN BOTH DBFBI TOPOLOGIES AND THE H-BRIDGE TOPOLOGY

	NPC	Series-switch	Series-diode	H-bridge
u_{S1}, u_{S2}	U_{dc}	$0.5U_{dc}$	U_{dc}	U_{dc}
u_{S3}, u_{S4}	$0.5U_{dc}$	$0.5U_{dc}$	$0.5U_{dc}$	U_{dc}
u_{S5}, u_{S6}	U_{dc}	U_{dc}	U_{dc}	$0.5U_{dc}(S_5)$
u_{D1}, u_{D2}	U_{dc}	U_{dc}	$0.5U_{dc}$	$0.25U_{dc}$
u_{D3}, u_{D4}	U_{dc}	$0.5U_{dc}$	U_{dc}	$0.25U_{dc}$

$$\begin{cases} d_{S1} = (2u_g / U_{dc}) - 1 & u_g > 0.5U_{dc} \\ d_{S2} = (-2u_g / U_{dc}) - 1 & -u_g > 0.5U_{dc} \\ d_{S3} = 2u_g / U_{dc} & 0 < u_g < 0.5U_{dc} \\ d_{S4} = -2u_g / U_{dc} & -0.5U_{dc} < u_g < 0 \end{cases} \tag{10}$$

From the above operation analysis, there is no current flowing through the body diodes of the switches. Therefore, compared with the conventional five-level H-bridge inverter topology shown in Fig.2, the presented five-level DBFBI topologies are free of reverse recovery problem in the freewheeling mode, and the MOSFETs with low on-resistances can be used instead of IGBTs. In addition, compared with the three-level DBFBI topology, the voltage jump of each high-frequency switch in the presented five-level DBFBI topology is only half of the input voltage. Therefore, the switching loss of the presented five-level DBFBI topology is much lower than that of the three-level DBFBI topology. Furthermore, the voltage jump of each inductor in the presented five-level DBFBI topology is only half of the input voltage as well, which means this topology features smaller filter inductance.

B. Analysis of Voltage Stress

The maximum drain-source voltages on the switches, S_5 and S_6, are equal to U_{dc}. The maximum reverse blocking voltages on the diodes, D_1 and D_2, are equal to U_{dc} as well. The switch S_1 is series connected with the switch S_3, and the switch S_2 is series connected with the switch S_4. Therefore, the maximum drain-source voltages on the switches, S_1, S_2, S_3 and S_4, are equal to $0.5U_{dc}$. The maximum reverse blocking voltages on the diodes, D_3 and D_4, are equal to $0.5U_{dc}$ as well.

The analysis process on the maximum voltage stresses of the power devices in the other five-level DBFBI topologies is similar. The results are summarized in Table I.

From Table I, it can be seen that the maximum drain-source voltages on the switches, S_5 and S_6, are the same in five-level DBFBI topologies. However, the maximum drain-source voltages on the switches, S_1 to S_4, are equal to $0.5U_{dc}$ in the series-switch five-level DBFBI topology. Therefore, the hardware cost of the series-switch five-level DBFBI topology is the lowest among DBFBI topologies.

C. Analysis of Neutral Point Potential Balancing

From Fig.8, both the switching state #2 and switching state #5 affect the NP potential of input split capacitors. During State #2, the voltage of C_{dc1} is increasing, and the voltage of C_{dc2} is decreasing. During State #5, the voltage of C_{dc1} is decreasing, and the voltage of C_{dc2} is increasing.

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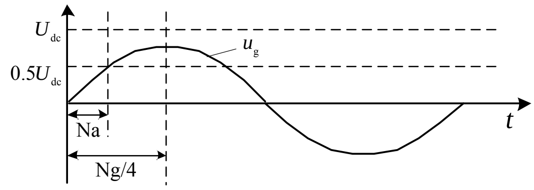

Fig.9. The sketch diagram of the switching times.

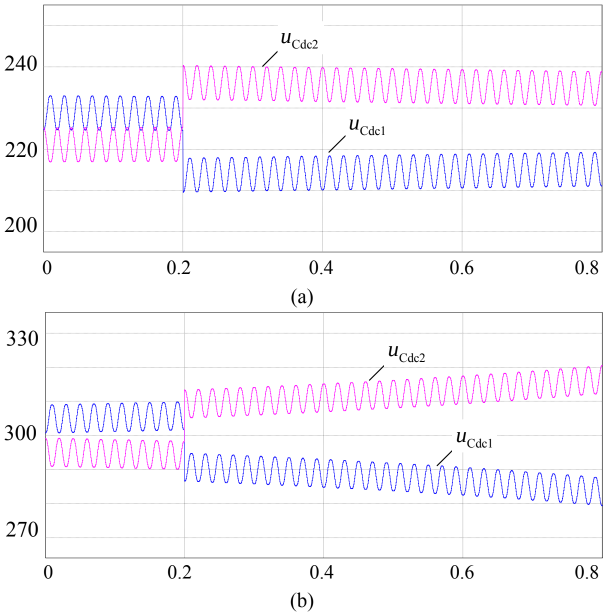

Fig.10. Simulation results of input capacitor voltages. (a) M= 0.591, U_{dc} = 550V. (b) M=0.541, U_{dc} = 600V.

At the positive half cycle of the utility grid, the voltage variation of C_{dc2} is represented as.

$$\begin{cases} \Delta u_{C2\text{-}1} = \dfrac{-i_{C2}}{C_{dc2}}(1-d_{S1})T_s & u_g > \dfrac{U_{dc}}{2} \\ \Delta u_{C2\text{-}2} = \dfrac{-i_{C2}}{C_{dc2}} d_{S3} T_s & 0<u_g < \dfrac{U_{dc}}{2} \end{cases} \tag{11}$$

where d_{S1} is the duty cycle of the switch S_1, and d_{S3} is the duty cycle of the switch S_3.

From (3), (4), (7), and (8), i_{L1} is calculated by u_{Cdc2} during the positive half cycle of the utility grid, and i_{L2} is calculated by u_{Cdc1} during the negative half cycle of the utility grid. Assuming that u_{Cdc1} is lower than u_{Cdc2}, the root mean square value of i_{L1} is larger than that of i_{L2}. Therefore, the feedback of inductor current will have a positive dc component, and the output of the inductor current regulator has a negative dc component. The modulation signal has a negative dc component as well. Hence, both the d_{S1} and the d_{S3} become smaller at the positive half cycle of the utility grid. The sum of $\Delta u_{C2\text{-}1}$ and $\Delta u_{C2\text{-}2}$ are obtained as,

$$\begin{cases} \sum\limits_{t=\mathrm{Na}+1}^{\mathrm{Ng}/4} \Delta u_{C2\text{-}1} = \dfrac{-2T_s}{C_{dc2}} \sum\limits_{t=\mathrm{Na}+1}^{\mathrm{Ng}/4} i_{C2}(t)(1-d_{S1}(t)) & u_g > \dfrac{U_{dc}}{2} \\ \sum\limits_{1}^{\mathrm{Na}} \Delta u_{C2\text{-}2} = \dfrac{-2T_s}{C_{dc2}} \sum\limits_{1}^{\mathrm{Na}} i_{C2}(t) d_{S3}(t) & 0<u_g < \dfrac{U_{dc}}{2} \end{cases} \tag{12}$$

where Ng represents the total switching times in a grid period, and Ng is defined as,

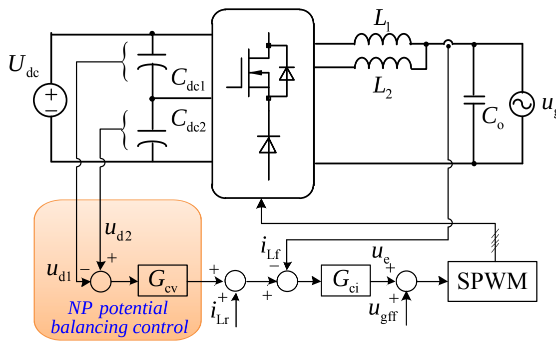

Fig.11. Control block of five-level DBFBIs.

$$\mathrm{Ng} = f_s / f_g \tag{13}$$

where f_g represents the frequency of the utility grid, and f_s represents the switching frequency.

Na represents the switching times in a quarter of grid period when $0 < u_g < 0.5U_{dc}$, as shown in Fig.9.

Na is defined as,

$$\mathrm{Na} = \mathrm{asin}\left(\frac{U_{dc}}{2U_{om}}\right) \cdot \frac{2}{\pi} \cdot \mathrm{Ng} \tag{14}$$

where U_{om} is the maximum amplitude voltage of the utility grid.

The modulation index of the five-level DBFBI topology can be calculated as

$$M = \frac{1}{2\sin\left(\dfrac{4\mathrm{Na}}{\mathrm{Ng}} \cdot \dfrac{\pi}{2}\right)} \tag{15}$$

If the sum of $\Delta u_{C2\text{-}1}$ is higher than the sum of $\Delta u_{C2\text{-}2}$, the decrease of u_{Cdc2} becomes larger at the positive half cycle of the utility grid. Therefore, the NP potential balancing can be realized without any additional control. Contrarily, if the sum of $\Delta u_{C2\text{-}1}$ is smaller than the sum of $\Delta u_{C2\text{-}2}$, the NP potential will be imbalanced.

Assuming that the voltage of the utility grid is 230V, and the frequency of the utility grid is 50Hz. The grid-tied power is 1kW, and the switching frequency is 40kHz.The NP potential balancing can be realized when M > 0.56. The simulation results are shown in Fig.10.

From Fig.10, it can be seen that when the modulation index is higher than 0.56, the divided input capacitor voltages are kept at self-balance. When the modulation index is lower than 0.56, the divided input capacitor voltages are imbalanced, and the voltages should be regulated by additional NP potential balancing mechanism, as shown in Fig.11, where u_{d1} and u_{d2} represent the voltage of C_{dc1} and C_{dc2}, respectively. i_{Lr} is the inductor current reference, and i_{Lf} is the feedback of the inductor current. u_{gff} represents the feed-forward component of the utility grid voltage. G_{cv} is the NP potential balancing regulator, and G_{ci} represents the inductor current regulator. The NP potential balancing is achieved by adding the output of NP potential balancing regulator and the inductor current reference.

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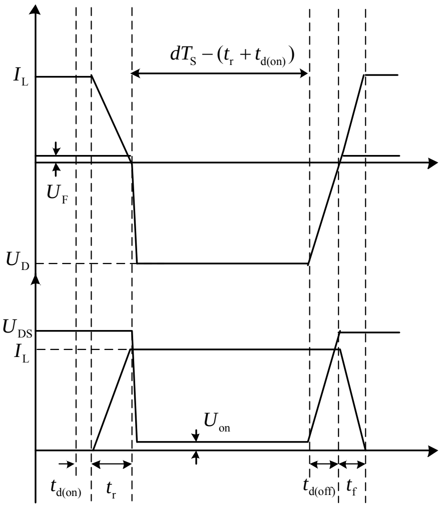

Fig.12. Hard-switching waveforms of MOSFETs for loss calculation.

IV. Calculation and Comparison of the Device Losses of Three Five-level Topologies

Power device losses are calculated based on the unified circuit parameters (given in Table III), and the device losses of the three-level DBFBI topology (part of Fig.5(a)) and three five-level DBFBI topologies (Fig.3.) are compared.

A. Power Losses of MOSFET Turn-on and Diode Turn-off

Fig.12 shows the waveforms for the turn-on transient of a MOSFET and the turn-off transient of a diode. Since the SiC diodes are used in DBFBI topologies, the power losses caused by the reverse recovery can be ignored. According to the data sheets of power devices, the turn-on behavior is characterized by using the rise time t_r. The turn-on loss of MOSFET is calculated as,

$$W_{\text{MOS,turn-on}}=\frac{1}{2}U_{\text{DS}}I_{\text{L}}t_{\text{r}} \quad (16)$$

where U_{DS} is the drain-source voltage of a MOSFET, I_L is the filter inductor current. For the three-level DBFBI topology, U_{DS} is equal to U_{dc}. For the five-level DBFBI topology, U_{DS} is equal to $0.5U_{dc}$.

The loss of diode turn-off can be calculated as,

$$W_{\text{Diode,turn-off}}=\frac{1}{2}U_{\text{F}}I_{\text{L}}t_{\text{r}} \quad (17)$$

where U_F is the ON-state voltage of the diode.

B. Power Losses of MOSFET Turn-off and Diode Turn-on

As shown in Fig.12, the turn-off of MOSFET and the turn-on of diode are also characterized by using the turn-off delay time t_d and the fall time t_f of MOSFET. The turn-off loss of MOSFET is calculated as,

$$W_{\text{MOS,turn-off}}=\frac{1}{2}U_{\text{DS}}I_{\text{L}}(t_{\text{f}}+t_{\text{d(off)}}) \quad (18)$$

The turn-on loss of diode can be calculated as,

$$W_{\text{Diode,turn-on}}=\frac{1}{2}U_{\text{F}}I_{\text{L}}t_{\text{f}} \quad (19)$$

C. On-state Power Losses for MOSFET and Diode

The conduction losses of MOSFET and diode can be calculated as,

$$W_{\text{MOS,on-state}}=I_{\text{L}}^{2}R_{\text{ds(on)}}(dT_{\text{S}}-t_{\text{r}}-t_{\text{d(on)}}) \quad (20)$$

$$W_{\text{Diode,on-state}}=U_{\text{F}}I_{\text{L}}((1-d)T_{\text{S}}-t_{\text{f}}-t_{\text{d(off)}}) \quad (21)$$

where $R_{ds(on)}$ is the on-state resistance of a MOSFET, d is the duty cycle of MOSFET, $t_{d(on)}$ is the turn-on delay time, and T_S is the switching period.

D. Gate Drive loss for MOSFET

The gate drive losses of MOSFETs are calculated as,

$$W_{\text{MOS,drive}}=Q_{\text{g}}U_{\text{gs}}f_{\text{s}} \quad (22)$$

where Q_g is the gate charge, U_{gs} is the drive voltage, and f_s is the switching frequency

E. Calculation Results

The series-switch five-level DBFBI topology is taken as an example for analysis. At the positive half cycle of the utility grid, the switches S_1, S_3, and S_6 are operating, while the diodes D_1 and D_3 are operating.

From Fig.7, the switch S_1 is operating with high frequency when $u_g > 0.5U_{dc}$. Therefore, the power loss of the switch S_1 is calculated as,

$$\begin{aligned}P_{\text{S1,loss}}&=\frac{\text{Ng/2-2Na}}{\text{Ng}}W_{\text{MOS,drive}}(i)\\&+\frac{2}{T_{\text{g}}}\sum_{i=\text{Na}+1}^{\text{Ng/4}}\left(\text{W}_{\text{MOS,on-state}}(i)+\text{W}_{\text{MOS,turn-on}}(i)+\text{W}_{\text{MOS,turn-off}}(i)\right)\end{aligned} \quad (23)$$

The switch S_3 is operating with high frequency when $u_g < 0.5U_{dc}$, and the switch S_3 is turned ON when $u_g > 0.5U_{dc}$. Therefore, the power loss of the switch S_3 is calculated as,

$$\begin{aligned}P_{\text{S3,loss}}&=\frac{2}{T_{\text{g}}}\sum_{i=1}^{\text{Na}}\left(\text{W}_{\text{MOS,on-state1}}(i)+\text{W}_{\text{MOS,turn-on}}(i)+\text{W}_{\text{MOS,turn-off}}(i)\right)\\&+\frac{2}{T_{\text{g}}}\sum_{i=\text{Na}+1}^{\text{Ng/4}}\text{W}_{\text{MOS,on-state2}}(i)+\frac{2\text{Na}}{\text{Ng}}W_{\text{MOS,drive}}(i)\end{aligned} \quad (24)$$

$W_{\text{MOS,on-state1}}(i)$ and $W_{\text{MOS,on-state2}}(i)$ are obtained as,

$$\begin{cases}W_{\text{MOS,on-state1}}=I_{\text{L}}^{2}R_{\text{ds(on)}}(d_{\text{S3}}T_{\text{S}}-t_{\text{r}}-t_{\text{d(on)}})\\W_{\text{MOS,on-state2}}=I_{\text{L}}^{2}R_{\text{ds(on)}}T_{\text{S}}\end{cases} \quad (25)$$

where d_{S1} is the duty cycle of S_1, and d_{S3} is the duty cycle of S_3.

The switch S_6 is ON during the positive half period of the utility grid, and the drive loss of the switch S_6 is ignored. Therefore, the power loss of S_6 is calculated as,

$$P_{\text{S6,loss}}=\frac{2}{T_{\text{g}}}\sum_{i=1}^{\text{Ng/4}}I_{\text{L}}^{2}(i)R_{\text{ds(on)}}T_{\text{S}} \quad (26)$$

The power loss of D_1 is calculated as,

$$P_{\text{D1,loss}}=\frac{2}{T_{\text{g}}}\sum_{i=1}^{\text{Na}}\left(\text{W}_{\text{Diode,on-state}}(i)+\text{W}_{\text{Diode,turn-on}}(i)+\text{W}_{\text{Diode,turn-off}}(i)\right) \quad (27)$$

The power loss of D_3 is calculated as,

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TABLE II.
TOTAL POWER DEVICE LOSSES OF SEVERAL TOPOLOGIES UNDER DIFFERENT SWITCHING FREQUENCIES

Switching frequency	20kHz (W)	30kHz (W)	40kHz (W)	50kHz (W)
Three-level DBFBI (TL)	7.52	8.89	10.25	11.63
NPC five-level (NPC-FL)	7.70	8.29	8.85	9.44
Series-switch five-level (SS-FL)	7.34	7.70	8.07	8.43
Series-diode five-level (SD-FL)	8.11	8.69	9.27	9.86
Three-level DBFBI (TL)	7.52	8.89	10.25	11.63

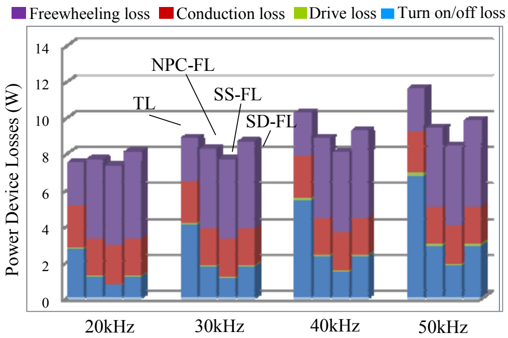


Fig.13. Total power device loss distributions of four DBFBI topologies under different switching frequencies.

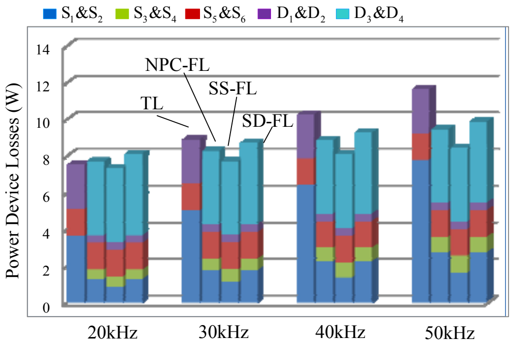


Fig.14. Device losses distribution of four DBFBI topologies under different switching frequencies.

$$P_{\mathrm{D3,loss}} = \frac{2}{T_{\mathrm{g}}}\sum_{i=\mathrm{Na}+1}^{\mathrm{Ng}/4}(W_{\mathrm{Diode,on-state1}}(i) + W_{\mathrm{Diode,turn-on}}(i) + W_{\mathrm{Diode,turn-off}}(i)) + \frac{2}{T_{\mathrm{g}}}\sum_{i=1}^{\mathrm{Na}} W_{\mathrm{Diode,on-state2}}(i) \quad (28)$$

$W_{\mathrm{Diode,on-state1}}(i)$ and $W_{\mathrm{Diode,on-state2}}(i)$ are obtained as,

$$\begin{cases} W_{\mathrm{Diode,on-state1}} = U_{\mathrm{F}} I_{\mathrm{L}}((1-d_{\mathrm{S1}})T_{\mathrm{S}} - t_{\mathrm{f}} - t_{\mathrm{d(off)}}) \\ W_{\mathrm{Diode,on-state2}} = U_{\mathrm{F}} I_{\mathrm{L}}(d_{\mathrm{S3}} T_{\mathrm{S}} - t_{\mathrm{r}} - t_{\mathrm{d(on)}}) \end{cases} \quad (29)$$

Since the power device losses at the positive half period of the utility grid are equal to the power losses at the negative half period, the total power device losses can be calculated as,

$$P_{\mathrm{total,loss}} = 2\cdot(P_{\mathrm{S1,loss}} + P_{\mathrm{S3,loss}} + P_{\mathrm{S6,loss}} + P_{\mathrm{D1,loss}} + P_{\mathrm{D3,loss}}) \quad (30)$$

F. Comparisons between the three-level DBFBI topology and the proposed five-level DBFBI Topologies

The power device losses of the three-level DBFBI topology and the five-level DBFBI topologies with the same parameters (as listed in Table III) are calculated, and the calculation processes are similar. Total power device losses of these topologies under different switching frequencies are listed in Table II.

In Table II, TL represents the three-level DBFBI topology, NPC-FL represents the NPC five-level DBFBI topology, SS-FL represents the series-switch five-level DBFBI topology, and SD-FL represents the series-diode five-level DBFBI topology. From Table II, it can be seen that the semiconductor loss of the series-switch five-level DBFBI topology is the lowest under different switching frequencies.

The semiconductor loss distributions of the three-level DBFBI topology and the proposed five-level DBFBI topologies are shown in Fig.13. It can be seen that there are almost no reverse recovery losses due to the use of SiC diodes. SS-FL has the lowest turn on/off losses and TL has the highest turn on/off losses. When the switching frequency is larger than 20kHz, the power device losses of five-level DBFBI topologies are dramatically less than those of the three-level DBFBI topology. The benefits on efficiency enhancements of the five-level DBFBI topologies become more obvious as the switching frequency increases.

The device loss distributions of these four topologies under different switching frequencies are shown in Fig.14. It can be seen that, the thermal stress distributions of power switches in these three five-level DBFBI topologies are almost the same. Furthermore, since the $u_{\mathrm{AB-n}}$ waveforms of the three five-level DBFBI topologies are the same, the filter inductor losses of the three five-level DBFBI topologies, with the same output power, the same inductor current ripple and the same switching frequency, are the same. Therefore, the inductor power losses of the three five-level DBFBI topologies are not calculated. However, compared with the three-level DBFBI topology, both the value and the volume of filter inductors in the five-level DBFBI topologies are smaller. Therefore, the inductor loss of proposed five-level DBFBI topologies is smaller than that of the three-level DBFBI topology.

V. EXPERIMENTAL RESULTS

A universal prototype was built up to verify the feasibilities of the three-level DBFBI inverter (part of Fig.5(a)), the NPC five-level DBFBI (Fig.3.), the series-switch five-level DBFBI (Fig.3(b)), the series-diode five-level DBFBI (Fig.3(c)), and the conventional five-level H-bridge inverter (Fig.2), and compare their performances. The specifications of these inverter topologies are listed in Table III. Since the lowest voltage rating of commercial SiC diodes is 600V, only one kind of SiC diode was used in the five-level DBFBI topologies. The control circuit was implemented based on a DSP chip TMS320F2808. In order to make a trade-off between the power density and the efficiency, the switching frequency of these three inverters were set at 40kHz. The YOKOGAWA WT1800 power analyzer was used to measure the efficiencies of these inverters.

Fig.15 shows the picture of the universal prototype, and Fig.16 shows the picture of the inductors used in the three-level

TABLE III
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
Input voltage	350~450V
Grid voltage	230V/50Hz
Grid frequency	50Hz
Rated power	1kW
Switching frequency	40kHz
Three-level filter inductor L_1&L_2	4mH
Five-level filter inductor L_1&L_2	2mH
Filter Capacitor C_o	0.47uF
High-voltage MOSFET	SPW47N60C3(650V)

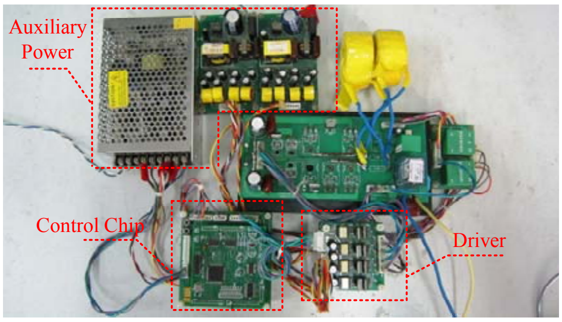


Fig.15 Picture of the universal prototype.

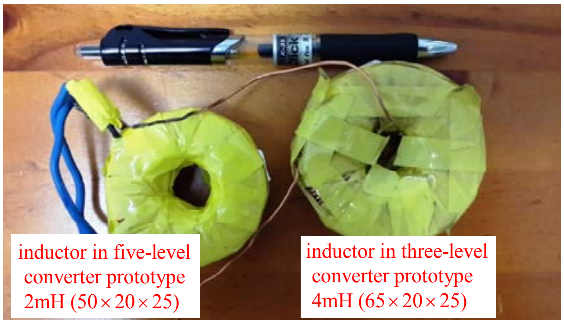


Fig.16 The filter inductors used in the three-level DBFBI and the five-level DBFBI.

DBFBI and the five-level DBFBI. The amorphous cores, which feature low high-frequency loss, were used as the magnetic material of filter inductors. From Fig.16, it can be seen that, the inductor volume in the five-level converter prototype is smaller than that in the three-level converter prototype. The outer diameter, inner diameter and height of the inductor in the three-level converter are 65mm, 20mm and 25mm respectively. While the outer diameter, inner diameter and height of the inductor in the five-level converter are 50mm, 20mm and 25mm respectively. Therefore, the five-level DBFBI topologies feature higher power density.

The experimental results of the series-switch five-level DBFBI are shown in Fig.17, where u_g and i_g represent the grid voltage and the grid-tied current respectively. u_{An} and u_{Bn} represent the voltages A to n and B to n respectively. u_{L1} and u_{L2} represent the voltages of filter inductors, L_1 and L_2, respectively. u_{S1}, u_{S2}, and u_{S3} represent the drain-source voltage on the switch S_1, the switch S_2, and the switch S_3, respectively. u_{D2} represents the reverse blocking voltage on D_2.

From Fig.17(a) it can be seen that, the series-switch five

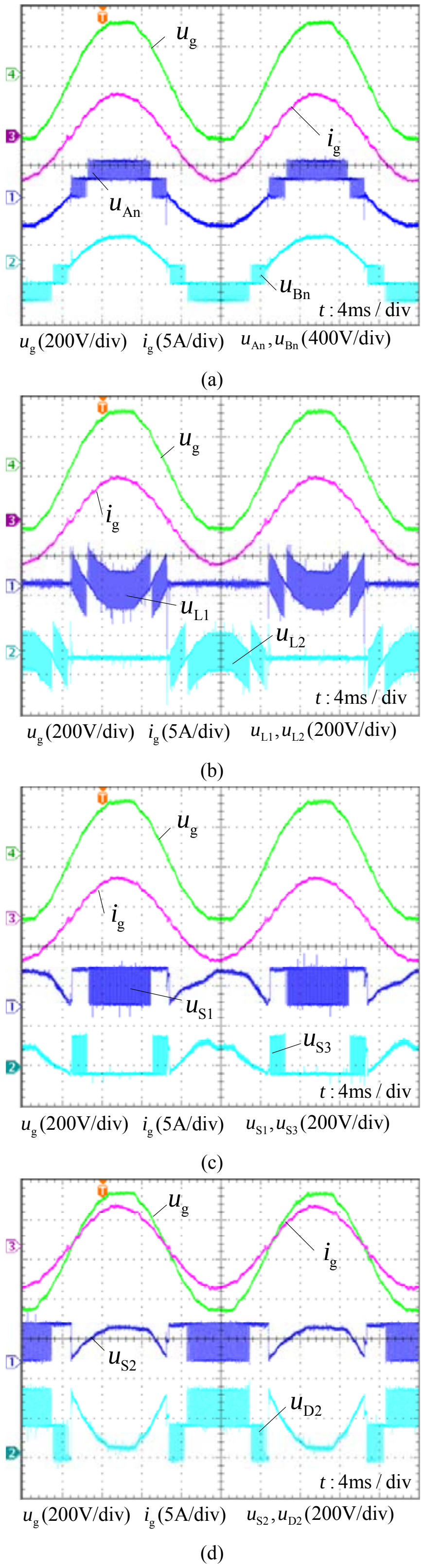
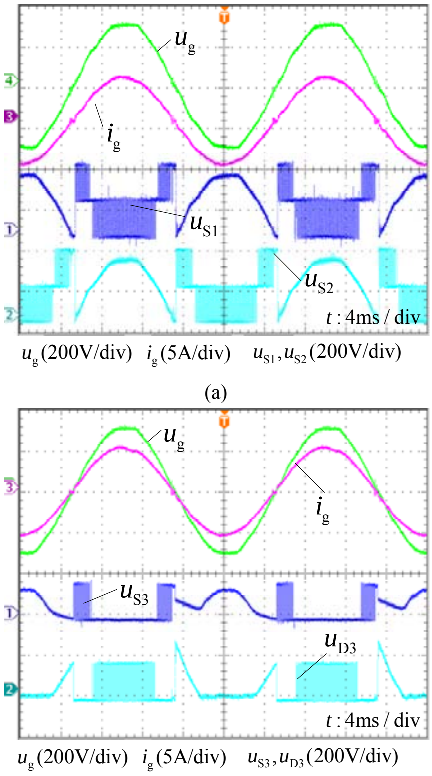


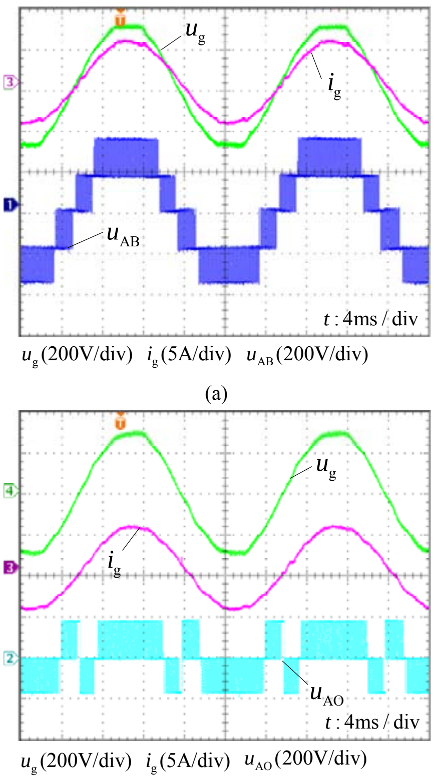
Fig.17. Experimental waveforms of the SS five-level DBFBI. (a) u_{An} and u_{Bn}. (b) voltages on filter inductors. (c) u_{S1} and u_{S3}. (d) u_{S2} and u_{D2}.

-level DBFBI operates with uniploar modulation, and the series-switch five-level DBFBI has five output voltage levels, U_{dc}, $0.5U_{dc}$, 0, $-0.5U_{dc}$, and $-U_{dc}$. The voltage jump of u_{AN} and



(b)

Fig.18. Experimental waveforms of the SD five-level DBFBI. (a) u_{S1} and u_{S2}. (b) u_{S3} and u_{D3}.



(b)

Fig.19. Experimental waveforms of the conventional five-level H-bridge inverter. (a) u_{AB}. (b) phase voltage.

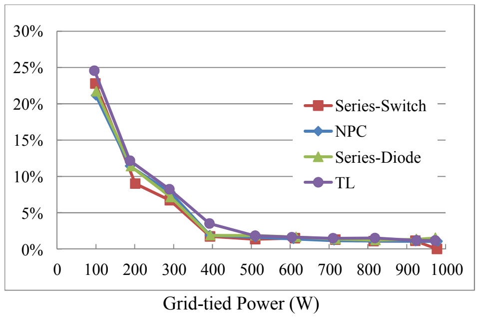


Fig.20. THD comparison of the three-level DBFBI and three proposed five-level DBFBI topologies.

u_{BN}, in the series-switch five-level DBFBI, is equal to half of the input voltage. From Fig.17(b) it can be seen that, the voltage jump of filter inductors in the series-switch five-level DBFBI is equal to half of the input voltage. Therefore, the five-level DBFBI topologies require smaller inductors than that of the three-level DBFBI topologies under the same switching frequency and output current ripple condition. From Fig.17(c), it can be seen that, both of the maximum drain-source voltages on S_1 and S_3 are equal to half of the input voltage, while the maximum reverse blocking voltage on D_2 is equal to the input voltage. This result verifies the analysis of voltage stresses in Section III. B.

The experimental results of the series-diode five-level DBFBI are shown in Fig.18, where u_{S1}, u_{S2}, and u_{S3} represent the drain-source voltage on the switch S_1, S_2, and S_3, respectively. u_{D3} represents the reverse blocking voltage on D_3.

From Fig.18(a), it can be seen that, both of the maximum drain-source voltages on S_1 and S_2 are equal to the input voltage, and the voltage jump of two switches are equal to half of the input voltage. From Fig.18(b), it can be seen that, the maximum drain-source voltage on S_3 is equal to half of the input voltage, while the maximum drain-source voltage on D_3 is equal to the input voltage. This result verifies the analysis of voltage stresses in Table I.

Experimental results of the conventional five-level H-bridge inverter are shown in Fig.19, where u_g and i_g are grid voltage and the grid-tied current. u_{AO} is the voltage of mid-point A to point O. u_{AB} is the voltage of A to point B.

From Fig.19(a) it can be seen that, the conventional five-level H-bridge inverter has five output voltage levels: U_{dc}, $0.5U_{dc}$, 0, $-0.5U_{dc}$, and $-U_{dc}$. From Fig.19(b) it can be seen that, the five-level H-bridge inverter operates with uniploar modulation.

The THD comparison of the three-level DBFBI, the NPC five-level DBFBI, the series-switch five-level DBFBI and the series-diode five-level DBFBI is shown in Fig.20.

Since the inductance of the three-level DBFBI topology is twice as much as that of proposed five-level DBFBI topologies, the THD performances of these topologies are almost the same. The THDs of these topologies are less than 5% when the grid-tied power is higher than 35% rated load.

Fig.21 shows the conversion efficiency comparison between the NPC five-level DBFBI and the five-level H-bridge inverter.

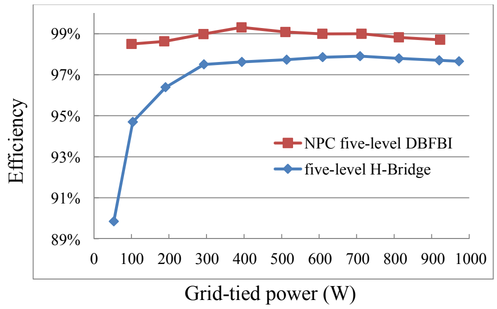


Fig.21. Efficiency comparison between the five-level H-bridge inverter and the proposed NPC five-level DBFBI.

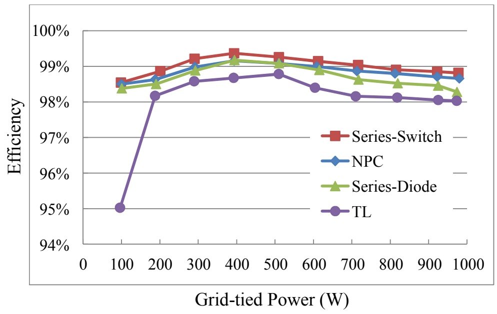


Fig.22. Efficiency comparison of the three-level DBFBI and three proposed five-level DBFBI topologies.

TABLE V.
COMPARISON OF CEC EFFICIENCIES

Topology	Efficiency
Three Level	98.21%
H-Bridge-Five Level	97.6%
Neutral Point Clamped-Five Level	98.89%
Switches-Series-Five Level	99.06%
Diode-Series-Five Level	98.72%

IGBTs are used in the conventional five-level H-bridge inverter, while MOSFETs and SiC diodes are used in the proposed NPC five-level DBFBI. It is obvious that the efficiency of the NPC five-level DBFBI is higher than that of the five-level H-bridge inverter within the whole load range. The NPC five-level DBFBI topology has no reverse recovery problem. Therefore, the efficiency of the five-level DBFBI topology has been dramatically enhanced by using the independent freewheeling diodes without reverse recovery losses and the power devices with low on-resistance.

The conversion efficiency comparison of the three-level DBFBI, the NPC five-level DBFBI, the series-switch five-level DBFBI and the series-diode five-level DBFBI is shown in Fig.22. It can be seen that, the series-switch five-level DBFBI topology exhibits the highest efficiency, and the efficiency of the NPC five-level DBFBI takes the second place. The efficiencies of these three five-level DBFBI topologies are higher than that of three-level DBFBI topology within the whole load range.

The California Efficiency Committee (CEC) efficiencies of the three-level DBFBI, the conventional five-level H-bridge inverter, the NPC five-level DBFBI, the series-switch five-level DBFBI, and the series-diode five-level DBFBI are listed in Table V.

From the above comparisons, experimental results of the conversion efficiency coincide with the theoretical analysis in Section IV. Hence, the five-level DBFBI topologies are good solutions for grid-tied inverters with high efficiency within a wide power range and high power density.

VI. CONCLUSION

The detailed derivation processes of two five-level full-bridge topology generation rules, including conventional full-bridge inverters and dual-buck full-bridge inverters, have been presented and explained. In order to enhance the reliability of five-level DBFBI topologies, an extended five-level DBFBI topology generation method has been proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter, and a family of five-level DBFBI topologies with high reliability has been generated. Furthermore, the relationship between the NP potential self-balancing and the modulation index of inverters are revealed.

Experimental results have verified that the five-level DBFBI topologies have the following advantages:

(1) Compared with the three-level DBFBI, the voltage jumps of high-frequency switching devices and the filter inductances are only half. Therefore, the family of five-level DBFBI topologies requires lower power rating devices and smaller filter inductors, which result in higher conversion efficiency and higher power density;

(2) The series-switch five-level DBFBI has the highest CEC efficiency compared with the three-level DBFBI, the conventional five-level H-bridge inverter, the NPC five-level DBFBI and the series-diode five-level DBFBI.

Hence, the family of five-level DBFBI topologies is an attractive solution for grid-tied renewable generation systems with high efficiency and high power density.

REFERENCES

[1] X. Guo, R. He, J. Jian, Z. Lu, X. Sun, Z. Lu, and J. M. Guerrero, “Leakage current elimination of four-leg inverter for transformerless three-phase PV systems,” *IEEE Trans. Power Electron*., vol. 31, no. 3, pp. 1841–1846, Mar. 2016.

[2] H. Wu, K. Sun, R. Chen, H. Hu, and Y. Xing, “ Full-Bridge three-port converters with wide input voltage range for renewable power systems,” *IEEE Trans. Power Electron*., vol. 27, no. 9, pp. 3965-3974, Sep. 2012.

[3] X. Wang, F. Blaabjerg, M. Liserre, Z. Chen, J. He, and Y. W. Li, “An active damper for stabilizing power-electronics-based AC systems,” *IEEE Trans. Power Electron*., vol. 29, no. 7, pp. 3318-3329, July. 2014.

[4] Y. Gu, Y. Wang, X. Xiang, W. Li, and X. He, “Improved Virtual Vector Control of Single-Phase Inverter for Dynamic Enhancement Based on Unified Model,” *IEEE Trans. Energy Convers*., vol. 29, no.3, pp. 611 - 618, Sep. 2014.

[5] X. Guo, D. Xu, and B. Wu, “Common-mode voltage mitigation for back-to-back current-source converter with optimal space-vector modulation,” *IEEE Trans. Power Electron*., vol. 31, no. 1, pp. 688–697, Jan. 2016.

[6] P. Sun, J-S. Lai, H. Qian, W. S. Yu, C. Smith, J. Bates, B. Arnett, A. Litvinov, and S. Leslie, “Efficiency evaluation of a 55kW soft-switching module based inverter for high temperature hybrid electric vehicle drives application,” in *Proc. 25th IEEE Appl. Power Electron. Conf. Expo*., Feb 2010, pp. 474-479.

[7] P. Sun, C. Liu, J-S. Lai, and C-L. Chen, “Cascade dual buck inverter with

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phase-shift control," *IEEE Trans. Power Electron*., vol. 27, no. 4, pp. 2067-2077, Apr. 2012.

[8] P. Sun, C. Liu, J-S. Lai, C-L. Chen, and N. Kees, "Three-phase dual-buck inverter with unified pulse width modulation," *IEEE Trans. Power Electron*., vol. 27, no. 3, pp. 1159-1167, Mar. 2012.

[9] P. Sun, C. Liu, J-S. Lai, and C-L. Chen, "Grid-tie control of cascade dual-buck inverter with wide-range power flow capability for renewable energy applications," *IEEE Trans. Power Electron*., vol. 27, no. 4, pp. 1839-1849, Apr. 2012.

[10] Z. Yao, L. Xiao, and Y. Yan, "Dual-buck full bridge inverter with hysteresis current control," *IEEE Trans. Ind. Electron*., vol. 56, no. 8, pp. 3153-3160, Aug. 2009.

[11] Z. Yao, L. Xiao, "Two-switch dual-buck grid-connected inverter with hysteresis current control," *IEEE Trans. Power Electron*., vol. 27, no. 7, pp. 3310-3318, Jul. 2012.

[12] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron*., vol. 57, no. 9, pp. 3118–3128, Sep. 2010.

[13] F. Hong, J. Liu, B. Ji, Y. Zhou, J. Wang, and C. Wang, "Single inductor dual buck full-bridge inverter," *IEEE Trans. Ind. Electron*., vol. 62, no. 8, pp. 4869–4877, Aug. 2015.

[14] B. Gu, J. Dominic, J-S. Lai, C-L. Chen, T. LaBella, and B. Chen, "High reliability and efficiency single-phase transformerless inverter for grid-connected photovoltaic systems," *IEEE Trans. Power Electron*., vol. 28, no. 5, pp. 2235-2245, May. 2013.

[15] B. Chen, B. Gu, L. Zhang, Z. U. Zahid, J-S. Lai, Z. Liao, and R. Hao, "A high-efficiency MOSFET transformerless inverter for noniolated microinverter applications," *IEEE Trans. Power Electron*., vol. 30, no. 7, pp. 3610-3622, Jul. 2015.

[16] J-M. Shen, H-L. Jou, J-C. Wu, and K-D. Wu, "Five-level inverter for renewable power generation system," *IEEE Trans. Energy Conv*., vol. 28, no. 2, pp. 257-266, Jun. 2013.

[17] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron*., vol. 57, no. 7, pp. 2219 - 2230, Jul. 2010.

[18] A. Nabae and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Appl*., vol. IA-17, no. 5, pp. 518 - 523, Sep./Oct. 1981.

[19] J. Mathew, P. P. Rajeevan, K. Mathew, N. A. Azeezm, and K. Gopakumar, "A multilevel inverter scheme with dodecagonal voltage space vectors based on flying capacitor topology for induction motor drives," *IEEE Trans. Power Electron*., vol. 28, no. 1, pp. 516-525, Jan. 2013.

[20] J. Rodriguez, J-S. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, control and applications," *IEEE Trans. Ind. Electron*., vol. 49, no. 4, pp. 724 - 738, Jul. 2002.

[21] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Trans. Ind. Electron*., vol. 60, no. 5, pp. 1907 - 1918, May. 2013.

[22] J. Li, J. Liu, D. Boroyecich, P. Mattavelli, and Y. Xue, "Three-level active neutral-point-clamped zero-current- transition converter for sustainable energy systems," *IEEE Trans. Power Electron*., vol. 26, no. 12, pp. 3680-3693, Dec. 2011.

[23] S-J. Park, F-S. Kang, M. H. Lee, and C-U. Kim, "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron*., vol. 18, no. 3, pp. 831-843, May. 2003.

[24] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for DC-AC conversion," *IEEE Trans. Power Electron*., vol. 21, no. 5, pp. 1311-1319, Sep. 2006.

[25] N. A. Rahim, and J. Selvaraj, "Multistring five-level with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron*., vol. 57, no. 6, pp. 2111-2123, Jun. 2010.

[26] J. Selvaraj, and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," *IEEE Trans. Ind. Electron*., vol. 56, no. 1, pp. 149-158, Jan. 2010.

[27] L. Zhang, N. Sun, and Y. Xing, "Grid connected five-level dual-buck full-bridge inverter with high-efficiency," *Proceeding of the Chinese Society of Electrical Engineering*., pp. 28-34, April, 2012. (in Chinese)

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